

22. The method according to claim 17, wherein  
said step of storing said second data is performed after said step of storing said  
first data.

B2  
end

23. The method according to claim 22, wherein said step of writing said  
second data is performed after said step of writing said first data.--

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REMARKS

Claims 1-12 have been allowed. Claims 13-17 have been rejected. Claims 18-23 are added. Care has been taken to avoid the introduction of new matter. Claims 1-23 are pending in this application.

The Office Action rejects claim 16 under 35 U.S.C. §112, second paragraph; claims 13-15 under 35 U.S.C. §102(e) as being anticipated by Otsuka [et al.] (U.S. Patent No. 6,154,393); and claims 16-17 under 35 U.S.C. §102(e) as being anticipated by Lee [et al.] (U.S. Patent No. 5,890,192). The rejections are respectfully traversed.

Rejection under 35 U.S.C. §112

The Examiner rejects claim 16, alleging that there is insufficient antecedent basis for the phrase "said first and second registers" in line 3. Claim 16 contains a typographical error and has been amended to recite "and first and second registers," which corrects the purported lack of antecedent basis. Withdrawal of the rejection is respectfully solicited.

Rejection of claims 13-15 under 35 U.S.C. §102(e)

The Examiner takes the position that Fig. 5 of Otsuka and associated text (col. 8, lines 21-43) discloses elements of claims 13-15. We respectfully disagree.

Otsuka is directed to improving device integrity of double data rate-mode (DDR-mode) comparable to single data rate-mode (SDR-mode) devices. Conventionally, integrity of DDR-mode devices is hampered by skew and RC delay of clock signals. Otsuka purports to reduce these problems thereby increasing device reliability.

The text at column 8 describes the DDR-mode operation of the circuitry of Fig. 5, and in particular, the text at lines 21-43 describes the reading operation of the device. As Otsuka explains, in a DDR-mode operation, an address signal is input to address register 2 and burst counter 4. The burst counter 4 generates a burst address signal. Sense amplifier 14 alternately reads data stored in a memory cell designated by the address signal and data stored in another memory cell designated by the burst address signal. (See col. 8, line 14 - 33). The read data is output via data lines DL1 to DL2 to the bus exchanger 16. Then, bus exchanger 16 alternately outputs data to the first output register 18 or second output register 20. Data stored by the first output register 18 is output in the first half of a clock cycle and data stored by the second output register 20 is output in the second half of the clock cycle. (See coll. 8, lines 34 - 43).

The preamble of claim 13 recites "A method for reading a plurality of data from a non-volatile semiconductor memory device...including a memory cell storing said plurality of data and a data output node for outputting said data..." In other words, claim 13 relates to a method for reading plurality of data from a single memory cell. As Otsuka explains, the DDR-mode operation is performed on two different memory cells from

which data corresponding to the address signal is read and data corresponding to the burst address signal is read, respectively. There is no disclosure or suggestion of data being read from the same memory cell as claim 13 recites.

For convenient reference, the steps of claim 13 are reproduced below.

reading a part of said plurality of data from said memory cell;  
outputting said part of said plurality of data to said output node;  
reading another part of said plurality of data from said memory cell; and  
outputting said another part of said plurality of data to said data output node.

As claim 13 recites, a part of the plurality of data is read from the memory cell which is output to the output node. Then, another part of the plurality of data is read from the same memory cell and is output to the data output node.

The Examiner seems to read the DDR-mode device's ability to output address-signal-designated data and burst-address-signal designated data on the steps recited by claim 13.

Otsuka relates to a DDR-mode device which is incapable of reading a plurality of data from a single memory cell part by part and outputting the read data part by part. Otsuka explains that the output address-signal-designated data and burst-address-signal designated data are selected from different memory cells. Otsuka also outputs the entire data selected by the address signal and the burst address signal. Otsuka does not disclose or suggest reading and outputting "a part" and "another part" of the plurality of data, as claim 13 recites.

Claim 14, dependent from claim 13, recites additionally that "said step of outputting said part of said plurality of data overlaps with said step of reading another part of said plurality of data." In the device of Otsuka, since data are collectively read out from a plurality of memory cells connected to identical word lines in the DRAM device,

the operational sequence as recited by claim 14 never occurs. Namely, the step of outputting the part of the plurality of data read from the memory cell never overlaps with the step of reading another part of the plurality of read data from the same memory cell.

Claim 15, an independent claim, relates to a method for reading data from a non-volatile semiconductor memory device, the device including "a word line, first and second bit lines, a first memory cell coupled to said word line and said first bit line, a second memory cell coupled to said word line and said second bit line, and a data output node for outputting said data from said first and second memory cells." It is noted that the first and second memory cell are coupled to the same word line.

Claim 15 recites the further steps of:

reading first data from said first memory cell with selectively activating said word line;  
outputting said first data to said data output node;  
reading second data from said second memory cell with selectively activating said word line; and  
outputting said second data to said data output node, wherein  
said step of outputting said first data overlaps with said step of reading second data.

It seems that the Examiner takes the position that the data output via data lines DL1 and DL2 read on features of claim 15 . However, as claim 15 recites, the first and second memory cells connect to a common word line. Otsuka explains that the address-signal-designated data and burst-address-signal designated data are read and output from different memory cells, but Otsuka does not disclose or suggest that the address-signal-designated data is output while the burst-address-signal designated data is read and vice-versa, as claim 15 would require.

As discussed previously in connection with claim 14, in Otsuka, since data are collectively read out from a plurality of memory cells connected to same word lines, the operational sequence of outputting data read from the memory cell never overlaps with the step of reading data in another memory cell. Claim 15, however, recites that "said step of outputting said first data overlaps with said step of reading second data." Otsuka, fails to disclose or suggest this feature.

For the above reasons, Otsuka fails to disclose or suggest the features of claims 13, 14, or 15. Withdrawal of the rejection is respectfully solicited. New dependent claims 18-21 are patentable at least based on their dependency to claims 13 or 15 and because the subject matter of the claims is not taught. In particular, claims 18-21 recite a unique order by which the steps of claim 15 are executed. The prior art of record fails to disclose or suggest such an order of execution.

Rejection of claims 16-17 under 35 U.S.C. §102(e)

The Examiner takes the position that Fig. 3 and associated text at column 4, lines 46-60, discloses claimed subject matter recited by claims 16-17. We respectfully disagree.

Lee addresses problems attendant time requirements for programming and verifying data chunks in EEPROM, which far exceed time requirements for providing address and data for each chunk of data. Lee purports to reduce chunk data write operation times. Fig. 3, to which the Examiner refers, schematically illustrates an EEPROM configured to operate with reduced chunk data write times. The Examiner particularly references col. 4, lines 46-60, as disclosing claimed subject matter. The cited

text provides that chunks of data are sequentially latched into first - fourth registers in response to latch enable signals and concurrently written into the respective subarrays.

In particular, with reference to Fig. 3 of Lee, the EEPROM system includes four sub-arrays 400-0 to 400-3. Each sub-array 400-0 - 400-3 connects to a respective data register Q(0) - Q(3). Sub-array pair 400-0 and 400-1 share a common row decoder (X-DEC) 401 and therefore share word lines. Sub-array pair 400-2 and 400-3 are similarly arranged. (See col. 4, lines 1-6). Data may be written to one of the first quadrant pair 400-0 - 400-1 concurrently with data written to one of the second quadrant pair 400-2 - 400-3. Each quadrant 400-0 - 400-3 is a distinct memory unit transmitting data between a respective data registers Q(0) - Q(3), but the pairs share a common row decoder.

As there is only one row decoder per sub-array, only one memory cell can be selected to receive data from a respective register. Moreover, since two quadrants share a row decoder, data is sequentially transferred from respective registers if the memory cell address for each quadrant are different.

Claim 16, an independent claim, relates to a method for writing data to a non-volatile semiconductor memory device, the "device including a memory cell storing first and second data, and first and second registers." Note that the preamble of claim 16 requires that a memory cell stores first and second data.

Claim 16 further recites steps of:

storing in said first register said first data input from the outside of said non-volatile semiconductor memory device;

writing said first data stored in said first register to said memory cell;

storing in said second register said second data input from the outside of said non-volatile semiconductor memory device; and

writing said second data stored in said second register to said memory cell.

The "storing" steps of claim 16 provide that the first data is stored in the first data register and the second data is stored in the second data register. The "writing" steps of claim 16, however, recite that the first data from the first register is written to the memory cell, and the second data from the second register is written to the same memory cell. In the Lee arrangement, only one register is associated with each quadrant. Lee does not disclose or suggest the method of claim 16 in which data from a first register is written to a memory cell and data from a second register is written to the same memory cell. Hence, claim 16 is patentable over the Lee reference.

Claim 16 recites additionally (in its preamble) "a memory cell storing first and second data, and first and second data registers." In order for a respective quadrant 400-0 - 400-3 to store first and second data, first data must be stored in the respective register and then written to the corresponding quadrant. After writing the first data, second data must be stored by the same register and then written to the corresponding quadrant.

Claim 17, dependent from claim 16, recites that "said step of writing said first data overlaps with said step of storing said second data." Lee discloses only one data register connecting to a respective quadrant, and therefore, is incapable having the overlap feature as claimed. Hence, claim 17 is patentable over the Lee reference.

For the above reasons, Lee fails to disclose or suggest the features of claims 16 and 17. Withdrawal of the rejection is respectfully solicited. New dependent claims 22 - 23 are patentable at least based on their dependency to claims 13 or 15. Furthermore, the subject matter of these dependent claims is not taught in the prior art of record. In

particular, the art of record fails to disclose or suggest the order of steps as the new claims recite.

In light of the remarks above, this application should be considered in condition with for allowance and passed to issue. If there are any questions regarding this amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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**APPENDIX SHOWING CHANGES MADE**

**IN THE CLAIMS:**

Claim 16 was amended as follows:

16. (Amended) A method for writing data to a non-volatile semiconductor memory device, said non-volatile semiconductor memory device including a memory cell storing first and second data, [said] and first and second registers, said method comprising the steps of:

storing in said first register said first data input from the outside of said non-volatile semiconductor memory device;

writing said first data stored in said first register to said memory cell;

storing in said second register said second data input from the outside of said non-volatile semiconductor memory device; and

writing said second data stored in said second register to said memory cell.